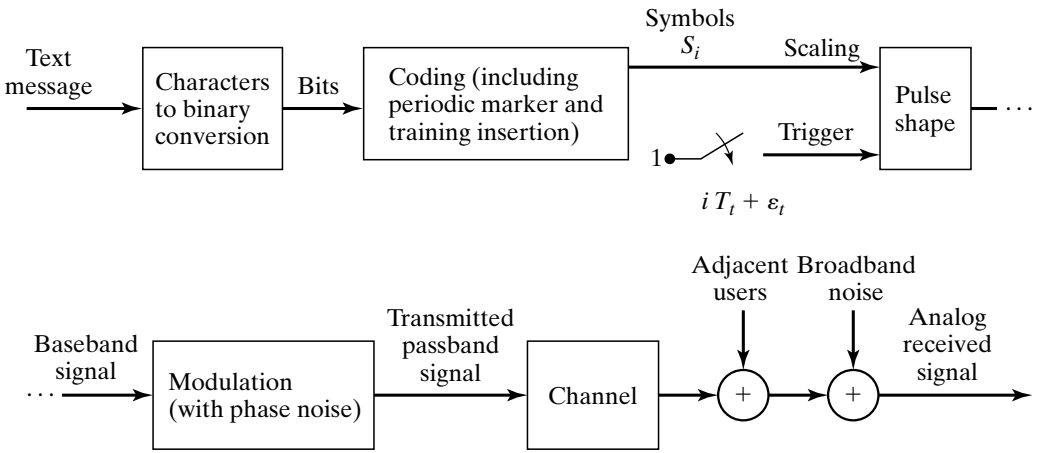
MIX'N'MATCH® RECEIVER DESIGN

- ⋆ Received Signal Construction
- ⋆ Receiver Design Methodolgy (in 4 Stages)
- ⋆ *Mix 'n' Match Mostly Marvelous Message Machine* ($\mathcal{M}^6$) Receiver Design Challenge

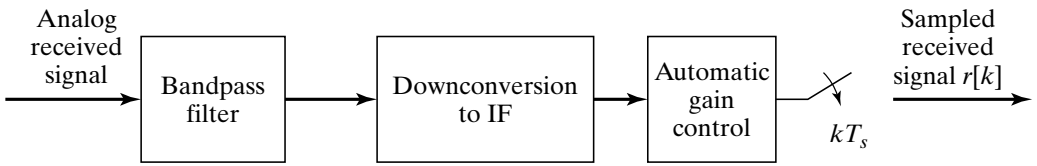
integration layer

Received Signal Construction

Receiver design responds to the received signal composition.
Transmitter and channel:



Receiver front-end:



Received Signal Construction (cont'd)

- Original character string message is coded into 7-bit ASCII format, coded with a (5,2) block code, and mapped to 4-PAM.
- Symbol sequence is composed as a 245-symbol marker/training segment, followed by 875 4-PAM message symbols, followed by the same 245-symbol marker/training segment, followed by another 875 message symbols, etc.
- Transmitter pulse period T_t not a precise match to the symbol period specification adopted by receiver.
- Transmitter pulse-firing trigger (or baud-timing) offset ϵ_t is unknown to receiver.
- Pulse shape is truncated SRRC with rolloff factor specified separately in range of 0.1 to 0.3 for each transmission.

Received Signal Construction (cont'd)

- Frequency division multiplexing slots exceed double half-power bandwidth of pulse shape.
- Transmitter carrier frequency closely, but not precisely, known at receiver.
- Transmitter carrier phase unknown to receiver and expected to be slowly wandering
- The channel can possess eye-closing ISI.
- Only the maximum delay spread of the potential ISI is known to the receiver in advance.
- Broadband noise is present, but modest.
- Narrowband interferers may be present as well.

Received Signal Construction (cont'd)

- Downconversion to IF by front-end will miss specified target frequency by only a small amount.
- Automatic gain control in front end is presumed converged and static.
- Sampler is free-running at a frequency well over twice the bandwidth of the pulse shape.
- Sampler is sub-Nyquist for IF, which means that downconversion will be performed on passband spectrum replica nearest baseband.

Received Signal Construction (cont'd)

Received Sampled Signal Specifications Table (left column):

symbol source alphabet
assigned intermediate frequency
nominal symbol period
SRRC pulse shape rolloff factor
FDM user slot allotment
truncated width of SRRC pulse shape
frame marker/training sequence
frame marker sequence recurrence period
time-varying IF carrier phase
IF frequency offset
transmitter baud timing offset
transmitter symbol period offset
channel delay spread maximum
sampler frequency

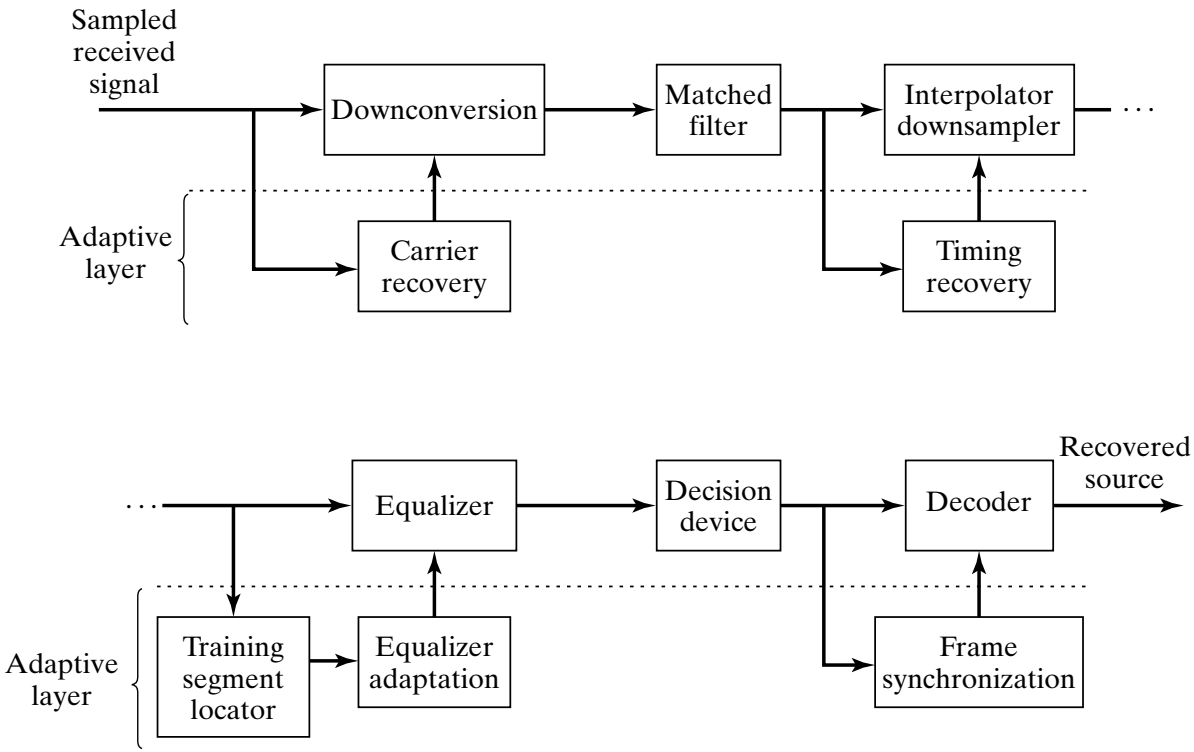
Received Signal Construction (cont'd)

Received Sampled Signal Specifications Table (right column):

± 1, ± 3
2 MHz
6.4 microseconds
$\beta \in [0.1, 0.3]$
204 kHz
8 transmitter clock periods
A0Oh well whatever Nevermind
1120 symbols
lowpass filtered white noise
fixed, less than 0.01% of assigned value
fixed
fixed, less than 0.01% of assigned value
7 symbols
850 kHz

Receiver Design Methodology

- Stage One: Ordering the basic operations
- Stage Two: Selecting components
- Stage Three: Countering anticipated impairments
- Stage Four: Tuning and testing



Design Methodology (cont'd)

Stage One: Ordering the basic components

- The basic receiver components are
  - downconversion with carrier recovery
  - baud-timing recovery with matched filter and interpolator/downsampler
  - trained equalizer with training segment locator
  - decision device and decoder with frame synchronization
- Our ordering (downconversion, timed downsampling, equalization, and decoding) is classical and popular but not the only possibility.

Design Methodology (cont'd)

Stage One: Ordering the basic components (cont'd)

- Timing and equalization can occur in the passband before carrier recovery.
- A fractionally-spaced equalizer can absorb the matched filter and resampling operations of the baud-timing component.
- Sometimes ordering is based on design tradeoffs at hand, sometimes on designer preference or personal experience, and sometime's on factors outside receiver designer's control (e.g. legacy product lines and intellectual property constraints).

Design Methodology (cont'd)

Stage Two: Selecting components

- Downconversion (like the other operations of basic components) can be done through many methods.
- Here the sub-Nyquist sampling of the IF signal places replicas closer to baseband.
- The closest is to be downconverted by a mixer (with an adapted phase) followed by a suitable lowpass filter.
- The presumption is that the components chosen, when properly tuned, result in acceptable performance.
- The proper operation of the components selected can be confirmed by simulations in an interference-free, ideal/full-knowledge setting.

Design Methodology (cont'd)

Stage Three: Countering anticipated impairments

- ○ residual interference from adjacent FDM band signals
- ○ AGC jitter
- ○ quantization noise in sampler
- ○ round-off noise in filters
- ○ residual interference from doubly upconverted spectrum
- ⊕ carrier phase jitter
- ⊕ baud timing jitter
- ⊕ residual MSE from equalizer
- ⊕ equalizer parameter jitter
- ⊕ noise enhancement by equalizer

[*Legend*: ⊕ major; ○ minor]

Design Methodology (cont'd)

Stage Three: Countering ... impairments (cont'd)

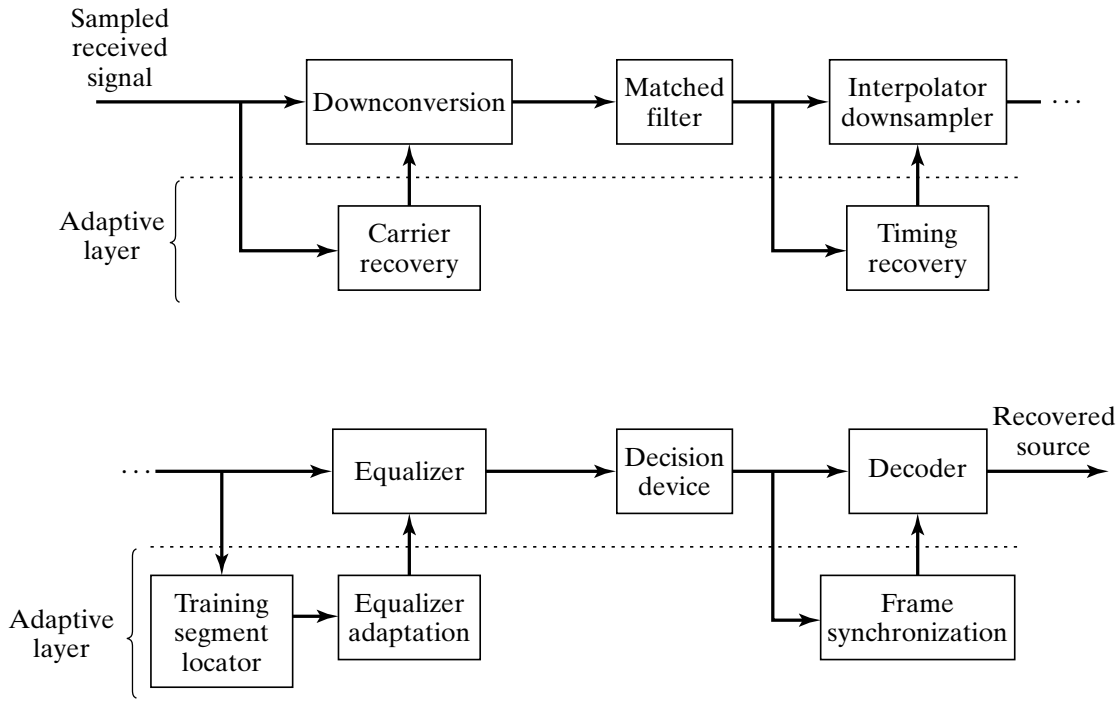
- We anticipate the need for
  - carrier phase adaptation
  - baud-timing adaptation
  - equalizer adaptation
  - post-decision frame synchronization
- Choices (so far)
  - Carrier phase recovery: squared difference, phase-locked loop, Costas loop, decision-directed
  - Baud-timing recovery on oversampled matched filter output: cluster variance or output power
  - Equalizer adaptation: trained LS, trained LMS, decision-directed, dispersion-minimizing
  - Frame synchronization: marker correlation

Design Methodology (cont'd)

Stage Four: Tuning and Testing

In order of appearance:

- Step One: Tuning the Carrier Recovery
- Step Two: Tuning the Clock Recovery
- Step Three: Tuning the Equalizer
- Step Four: Frame synchronization for decoder



Design Methodology (cont'd)

Stage Four: Tuning and Testing (cont'd)
Plan of action:

- One at a time
- In order of appearance
- With preceding steps countering their impairments as intended
- Each with its own share of total allowable error

Design Methodology (cont'd)

Stage Four: Tuning and Testing (cont'd)

Tuning tradeoffs:

- All adaptive components will select stepsize in tradeoff between rapid tracking and dampened jitter.
- Carrier recovery
  - dual or single-loop structure
  - LPF cutoff and range between in-band and stopband gain
- Clock recovery
  - δ in derivative
  - time support of interpolation filter

Design Methodology (cont'd)

Stage Four: Tuning and Testing (cont'd)

- Equalizer
  - number of taps: channel inverse delay spread; 2 to 5 times channel maximum delay spread
  - training signal delay: half of equalizer length
  - initialization: center spike
- Frame synchronization
  - marker chosen for peaky autocorrelation
  - preferred marker unlikely to occur in message

$\mathcal{M}^6$ Receiver Design Challenge

Your receiver should offer user opportunity for setting with each transmission

- SRRC rolloff factor
- initial phase offset
- initial timer offset
- initial equalizer parameterization

and work automatically after their specification...

$\mathcal{M}^6$ ... Challenge (cont'd)

Development Tips

- simulate transmitter to allow controlled tests on broader set of circumstances than provided by test signal set
- probe receiver limits (e.g. assess how much noise causes performance failure)
- implement debug mode that plots pertinent signals
- test an adaptive element in two scenarios:
  - (i) start at right answer with zero stepsize and see if achieved performance is as expected, and then
  - (ii) start near right answer with nonzero stepsize and see if algorithm shrinks into tight orbit about right answer